a second signal processor;

a first memory; and

a second memory;

said first signal processor having write access at any time to any location in said first memory and read access at any time to any location in said first memory and said second memory; and

said second signal processor having write access at any time to any location in said second memory and read access at any time to any location in said first memory and said second memory,

wherein said first and second signal processors operate independently of each other, and

wherein said first and second signal processors provide a first and second signal, respectively, to said master processor so as to notify said master processor that newly-written-in data can be obtained from one or both of said first and second memories.

11 ~~31.~~ (Twice Amended) An apparatus comprising a plurality of signal processors, a master processor, and a plurality of memories, each signal processor having write access at any time to only a particular one of said memories and read access at any time to any of said memories, wherein at least one of said signal processors in said plurality operates independently of other signal processors in said plurality of signal processors, and

wherein said signal processors provide a respective indication signal to said master processor so as to notify said master processor that newly-written-in data can be obtained from one or more of said plurality of memories.

12 ~~32.~~ (Amended) The apparatus recited in claim 11 ~~31~~, wherein said [first memory and said second memory] plurality of memories comprise respective portions of a same memory.

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Please add the following new claims:

--~~35.~~ 8 The apparatus recited in claim ~~23~~, 1 wherein said first signal processor provides said first signal to said master processor to notify said master processor that newly-written-in data into said first memory by said first signal processor can be obtained from said first memory, and

wherein said second signal processor provides said second signal to said master processor to notify said master processor that newly-written-in data into said second memory by said second signal processor can be obtained from said second memory.

~~36.~~ 9 The apparatus recited in claim ~~25~~, 8 wherein said master processor has write access and read access to each of said first and second memories.

~~37.~~ 10 The apparatus recited in claim ~~26~~, 9 wherein control of said first and second processors is always maintained by said master processor.

~~38.~~ 14 The apparatus recited in claim ~~31~~, 11 wherein said master processor has write access and read access to each of said plurality of memories.

~~39.~~ 15 The apparatus recited in claim ~~38~~, 14 wherein control of said plurality of processors is always maintained by said master processor.--